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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/494,953	02/01/2000	Yoshiharu Kato	P8075-9034	4157

7590 11/21/2002

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/494,953	KATO, YOSHIHARU	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. The Examiner withdraws all restriction requirements presented in the previous action. All claims 1-48 are examined in the current Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 12-14 and 19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner would like to point out that claim 11 from which claim 12 depends cites "a first output circuit connected to each bus line" which implies a single first output circuit connected to each bus. Claim 12 contradicts the implied single first output circuit by introducing a first output circuit corresponding to a selected bus lines and other first output circuits corresponding to other bus lines.

Claims 13, 14 and 19-21 cite similar language as in claim 12.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 18-21, 24-26, 28, 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama, Hideki (JP 05053857 A)

4. 35 U.S.C. 102(b) rejection of claims 18 and 25.

Akiyama teaches electronic device comprising first and second semiconductor devices connected (see LSI-A 10 and LSI-B 20 in Figure 1, Akiyama) to each other with a plurality of bus lines (see 103 and 104 in Figure 1, Akiyama), wherein the first semiconductor device includes (see LSI-A 10 in Figure 1, Akiyama): a first output circuit connected to each bus line for supplying each bus line with a first logical output signal (see test circuit 6 in Figure 1, Akiyama; Note: test circuit 6 in Figure 1 is connected to bus line 104 via test circuit 7), an inversion output circuit connected to each bus line for supplying each bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal (see inverter 1 in Figure 1, Akiyama), and a comparison circuit connected to each bus line (see comparator 5 in Figure 1, Akiyama); and the second semiconductor device (see LSI-B 20 in Figure 1, Akiyama) includes: an input circuit connected to each bus line for acquiring a first bus line signal (see test circuit 7 in Figure 1, Akiyama), and a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal (see test circuit 7 in Figure 1, Akiyama), wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and

the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device (see bus lines 107 & 108 and comparator 109, Akiyama).

5. 35 U.S.C. 102(b) rejection of claims 19-21.

See rejection to claims 18 and 25, above.

6. 35 U.S.C. 102(b) rejection of claim 24.

The Examiner would like to point out that claims 1, 6 and 11 cites similar language as claim 24 rejected above. In addition, the Examiner would like to point out line 104 caries a first logical output and line 105 caries a second (see Figure 1, Akiyama).

7. 35 U.S.C. 102(b) rejection of claims 26 and 28.

The Examiner would like to point out that test circuits 6 and 7 in Figure 1 of Akiyama are inherently latch circuits for latching transmitted test data since digital data requires clocked sequential circuitry (or latches) to buffer incoming data prior to processing.

8. 35 U.S.C. 102(b) rejection of claims 30 and 31.

See test circuits 6 and 7 and inverter 1 in figure 1 of Akiyama.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-17, 22, 23, 27, 29 and 32-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama, Hideki (JP 05053857 A).

10. 35 U.S.C. 103(a) rejection of claims 1, 6, 11 and 24.

The Examiner would like to point out that claims 1, 6 and 11 cites similar language as claims 18 and 25 rejected above, except as noted below.

However Akiyama, does not explicitly teach the specific use of an inverter in the second semiconductor device.

The Examiner would like to point out that that the purpose of the claimed invention of the Applicant's claim 1 and the teachings of Akiyama is to compare an inverted version of a test signal transmitted on a line to test for connectivity. Placement of inverters to

achieve this objective is an obvious Engineering Design choice as acknowledged by the Applicant in the Applicant's claim 8 which is an alternative embodiment of the invention claimed in the Applicant's claim 1 and which is substantially identical to the teachings in the Akiyama patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Akiyama patent by including use of an inverter in the second semiconductor device. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an inverter in the second semiconductor device would provide the opportunity implement an alternative embodiment of the method taught in the Akiyama patent based on Engineering Design choice.

11. 35 U.S.C. 103(a) rejection of claims 2, 4, 7 and 9.

The Examiner would like to point out that line 104 carries a first logical output and line 105 carries a second (see Figure 1, Akiyama).

12. 35 U.S.C. 103(a) rejection of claims 3 and 8.

Claims 3 and 8 cite the additional limitation, "a first bus line adjacent to a second bus line". The Examiner would like to point out that placement of bus lines is an Engineering Design choice. See rejection to claims 1, 6 and 11, above.

Claim 32 cites similar language.

13. 35 U.S.C. 103(a) rejection of claims 5, 10 and 12-14.

See rejection to claims 1, 6 and 11, above.

14. 35 U.S.C. 103(a) rejection of claims 15, 16, 22 and 23.

The Examiner would like to point out that test circuits 6 and 7 are the only output circuits for outputting data on lines 103 and 104 whether the data is test data or data generated under normal conditions (see Figure 1, Akiyama).

15. 35 U.S.C. 103(a) rejection of claims 17, 27 and 29.

See rejection to claims 26 and 28, above. In addition, test circuits 6 and 7 are connected to control lines 101, 102 and 111 (see Figure 1, Akiyama). Use of a reset signal for control would be an Engineering Design Choice, which does not deviate from the scope or the intent of the teachings in the Akiyama patent since Akiyama teaches control mechanisms for controlling test circuits 6 and 7, which encompass a particular embodiment such as a reset signal for controlling operation.

16. 35 U.S.C. 103(a) rejection of claim 32.

Akiyama, substantially teaches the claimed invention described in claims 30 and 31 (as rejected above).

However Akiyama, does not explicitly teach that the input logic circuit is physically located close to the input terminals, and the bus drive circuit is physically located close to the second bus line.

The Examiner would like to point out that placement of bus lines is an Engineering Design choice hence does not deviate from the scope or the intent of the teachings in the Akiyama patent (see rejection to claims 30 and 31, above).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Akiyama patent by placing the input logic circuit physically close to the input terminals, and the bus drive circuit physically close to the second bus line. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that placing the input logic circuit physically close to the input terminals, and the bus drive circuit physically close to the second bus line would provide the opportunity to implement the teachings in the Akiyama patent based on Engineering Design choice.

17. 35 U.S.C. 103(a) rejection of claims 33-46 and 48.

Claims 33-46 and 48 cite specific well-known circuits (such as clamps PMOS transistors, etc.) for implementing the method of claims 1-29 (rejected above) and are based on Engineering Design choice.

18. 35 U.S.C. 103(a) rejection of claim 47.

See rejection to claims 31-46 and 48,above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Okamoto, Yasushi et al. (US 5659548 A) teaches a communication control apparatus performing data communication control with a node of high priority occupying a bus by comparing echo back data with data transmitted from the node itself. Yajima, Noboru et al. (US 5367395 A) teaches a first apparatus, transmission signals are inverted in a sending side and are restored in a receiving side in one direction of two-way communication, and transmission signals are not inverted in another direction, to thereby distinguish a signal reflected at a fault point of an optical fiber from normal receiving signals from the station of the other party. Okazaki, Katsuyoshi (US 5193093 A) teaches a data transfer process for transferring data from a first system to a second system while carrying out loop checking.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133
November 10, 2002

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